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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/902,827

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Eric Mathew Trehus

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EXAMINER

WILSON, YOLANDA L

ART UNIT

PAPER NUMBER

2113

DATE MAILED: 02/05/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/902,827

Applicant(s)

TREHUS ET AL.

Examiner

Yolanda Wilson

Art Unit

2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1,5,6,7,8,9,11 are rejected under 35 U.S.C. 102(e) as being anticipated by Natsume et al. (USPN 6523138). As appears in claim 1, Natsume et al. discloses a set of at least two masters and at least one target in column 4, lines 19-23; at least one bus providing connection between the masters and the target in column 4, lines 26-28; a system controller operable to quiesce masters from the set of masters in response to an error message in column 9, lines 7-15; a system error processor operable to handle an error condition indicated by the error message in column 8, lines 66-67 – column 9, lines 1-6.

3. As per claim 5, Natsume et al. discloses the error message causing the system controller to quiesce the selected masters is programmable in column 8, lines 66-67 – column 9, lines 1-2.

4. As per claim 6, Natsume et al. discloses at least one means for receiving and providing data and a set of means for addressing the means for receiving and providing data in column 4, lines 19-23; a means for providing connection between the set of

means for receiving and providing data and the at least one means for addressing in column 4, lines 26-28; a means for quiescing masters from the set of masters in response to an error message in column 9, lines 7-15; a means for handling an error condition indicated by the message in column 8, lines 66-67 – column 9, lines 1-6.

5. As per claim 7, Natsume et al. discloses the error message causing the system controller to quiesce the selected masters may be programmable in column 8, lines 66-67 – column 9, lines 1-2.

6. As per claim 8, Natsume et al. discloses receiving an error message indicating an error condition has arisen, determining if the error message is one which triggers auto quiesce, and generating auto quiesce signals to stop operations in the selected masters in column 8, lines 66-67 – column 9, lines 1-2.

7. As per claim 9, Natsume et al. discloses re-enabling the selected masters after the error condition has been cleared column 9, lines 33-46.

8. As per claim 11, Natsume et al. discloses determining if the error message further is one which triggers auto quiesce further comprises preconfiguring a system controller with the error messages in column 8, lines 66-67 – column 9, lines 1-2.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Natsume et al. in view of Armany et al. (USPN 6412027B1). Natsume et al. fails to explicitly state the set of masters includes at least one direct memory access controller.

Armany et al. discloses the function of a DMA controller in column 1, lines 36-40, "As computing systems advanced, DMA controllers were created to facilitate such data transfers by controlling the movement of data directly from one memory device to another memory device."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the set of masters includes at least one direct memory access controller. A person of ordinary skill in the art would have been motivated to have the set of masters includes at least one direct memory access controller because DMA controllers are used to control the transfer of data from one device to another device.

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Natsume et al. in view of Potter (USPN 5608884A). As per claim 3, Natsume et al. fails to explicitly state the set of masters includes at least one peripheral component interconnect controller.

Potter discloses a PCI controller in column 2, lines 38-39, "Also residing on the local bus 15 is a peripheral connection interface (or "PCI") controller..."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the set of masters includes at least one peripheral component interconnect controller. A person of ordinary skill in the art would have been

motivated to have the set of masters includes at least one peripheral component interconnect controller because the PCI controller is used to control signals between devices on different buses. Potter discloses in column 2, lines 39-43, "(or "PCI") controller 18 which controls exchanges of address, data and control signals between devices residing on the local bus 15, for example, the CPU 14, and devices residing on a PCI bus 20 coupled to the local bus 15 by a bridge 22."

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Natsume et al. in view of Holm et al. (US Publication Number 20020152334). As per claim 4, Natsume et al. fails to explicitly state at least one bus includes a peripheral component interconnect bus.

Holm et al. discloses on page 1, paragraph 0005, "A peripheral component interconnect (PCI) bus is an industry standard IO bus that is widely used in computer systems ranging from typical desktop systems..."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have at least one bus includes a peripheral component interconnect bus. A person of ordinary skill in the art would have been motivated to have at least one bus includes a peripheral component interconnect bus because a PCI bus is used to transfer information between devices in a computer system. Holms et al. discloses on page 1, paragraph 0005, "The PCI IO bus implemented in these types of systems is generally in communication with a computer system central processing system (CPU) and/or memory complex via a PCI host bridge (PHB)."

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Natsume et al. in view of Berg et al. (USPN 6629184). As per claim 10, Natsume et al. fails to explicitly state the error message is an interrupt.

Berg et al. discloses in column 9, lines 55-60, "hard disk drive 20 immediately determines that 01h is an invalid command, and in response to this determination, generates an interrupt by asserting line INTRQ, and generates an error message by setting ERR in the status register and ABRT in the error register."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the error message be an interrupt. A person of ordinary skill in the art would have been motivated to have the error message be an interrupt because interrupts indicate that an error has occurred in the computer system. Berg et al. discloses in column 9, lines 60-64, "CPU 10 responds to the interrupt by reading the status register and detecting that ERR is set and then responds to ERR being set by reading the error register and detecting that ABRT is set. In this fashion, CPU 10 is informed that the write operation has not occurred."

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Natsume et al. in view of Yazdy (USPN 5815676). Natsume et al. fails to explicitly state signaling an address arbiter to halt address grants for the selected masters.

Yazdy discloses signaling an address arbiter to halt address grants for the selected masters in column 3, lines 60-67 – column 4, lines 1-2, "Exemplary embodiments of the present invention provide an address arbiter which handles split bus transactions... In addition to prioritizing requests from those bus masters, the

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address arbiter also handles two cases where the arbiter prevents any of the bus masters from acquiring the address bus."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an address arbiter to halt address grants for the selected masters. A person of ordinary skill in the art would have been motivated to store the solution to have an address arbiter to halt address grants for the selected masters because address arbiters are used to handle which devices can or cannot have access to an address bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.


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